



H61H2-M7

Rev : 1.0

ECS
CONFIDENTIAL

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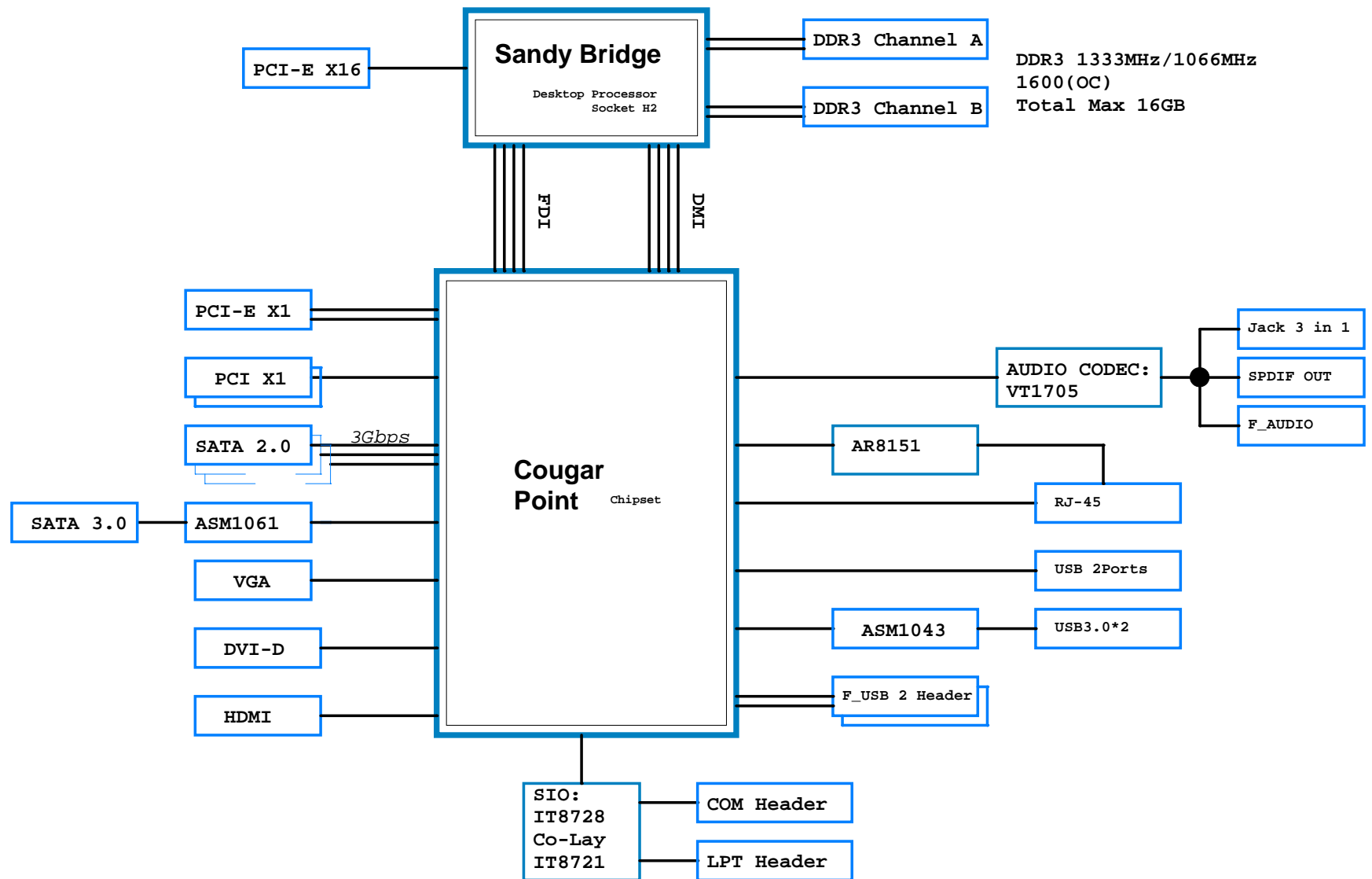
REVISION HISTORY:

Rev	Date	Notes
V A(H61H2-M)	2010/11/29	Initial version
V1.0(H61H2-M)	2011/02/18	1. fix can't boot issue 2. remove MOS heat sink 3. Add ME_Test for PV test 4. fix measure HDMI signal fail issue 5. fix 5VSB inrush current issue
V A(H61H2-M7)	2011/04/15	1. Delete TPM & 1394 2. Add SATA 3.0 ASM1061 3. Add HDMI 4. USB3LAN change to USBLAN 5. 2 Rear USB Ports & 2 Rear USB 3.0 Ports 6. ADD GPIO control V_DIMM Voltage 7. Change to 2 DIMMs 8. SYS_FAN change to 4-pin smart FAN
V 1.0(H61H2-M7)	2011/06/08	1. V_DIMM OCP RES change to 13.7K,30A 2. R16 & R31 change to 0 ohm

NOTE:

1. Model Code: EB5
2. Modified from H61H2-M V 1.0

 Elitegroup Computer Systems	
Title: Cover Page	
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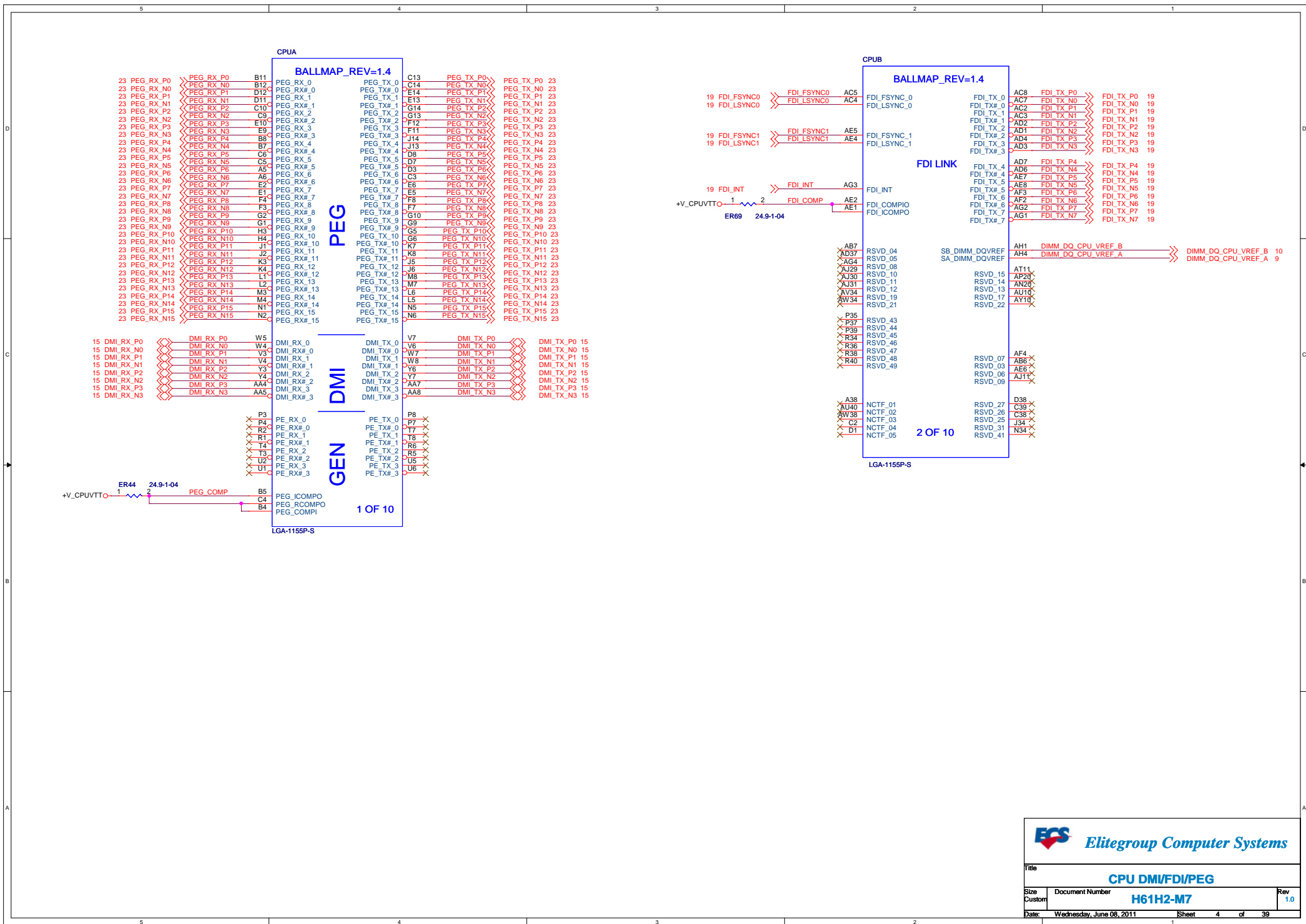


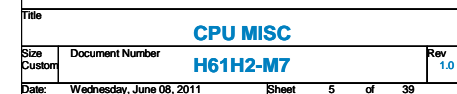
PCH-GPIO function

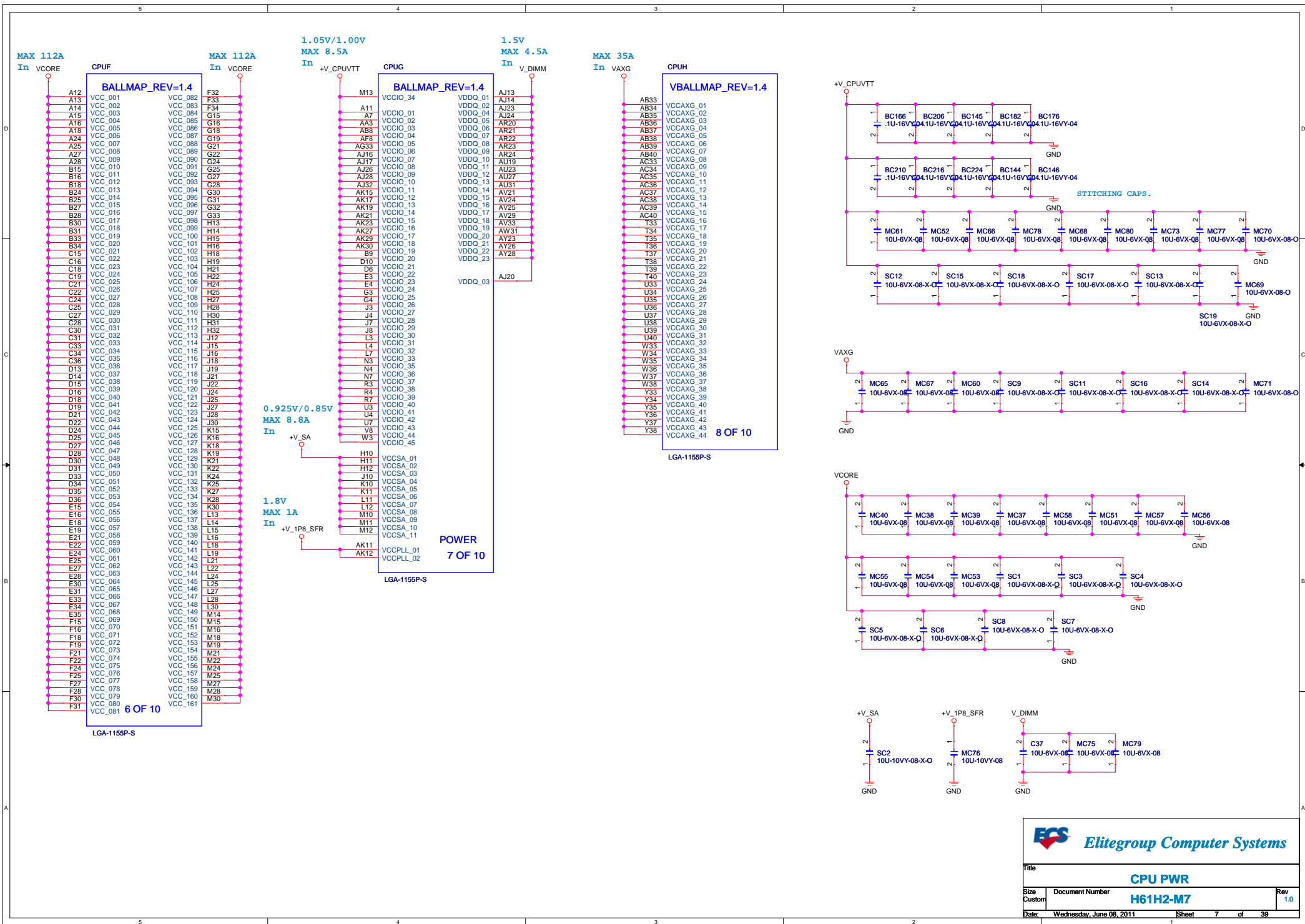
Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	VT1705CD/VT1705CE	GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

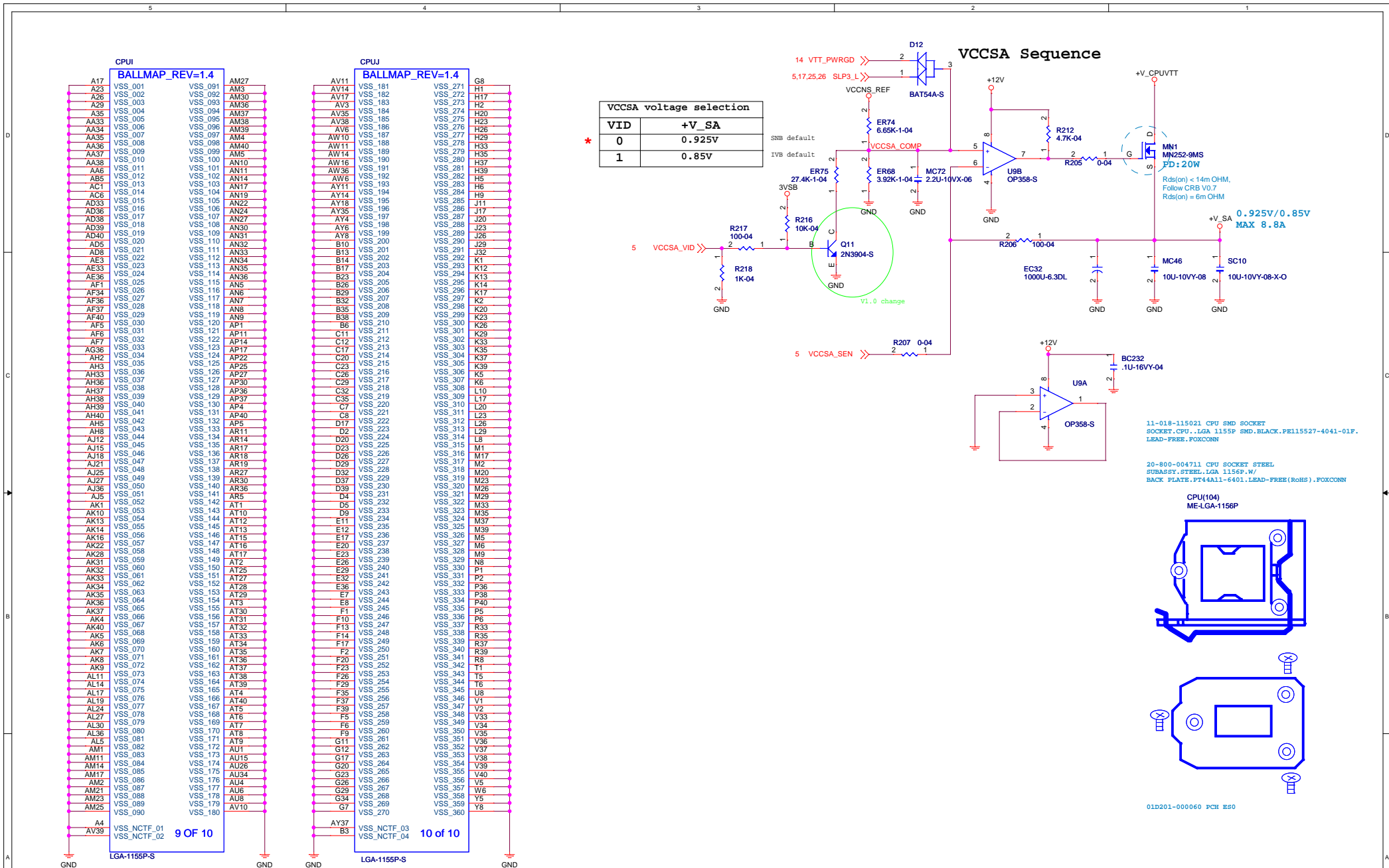
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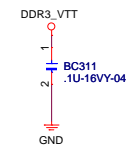
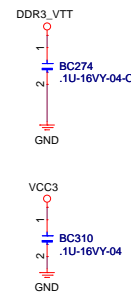
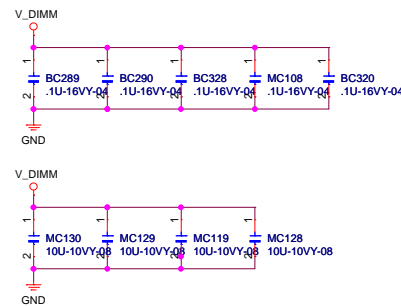
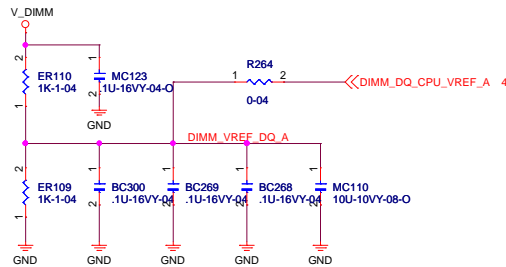
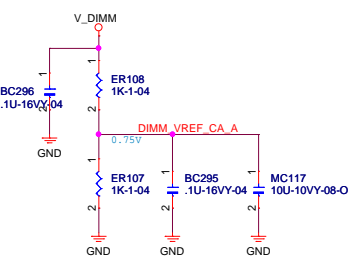
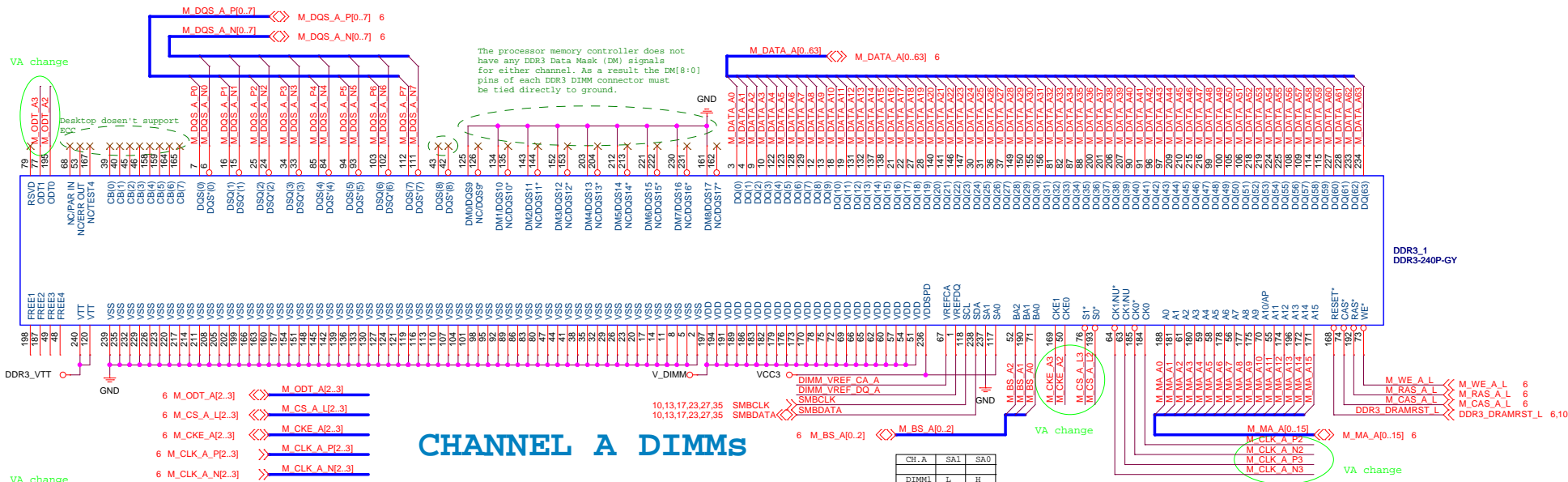
Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



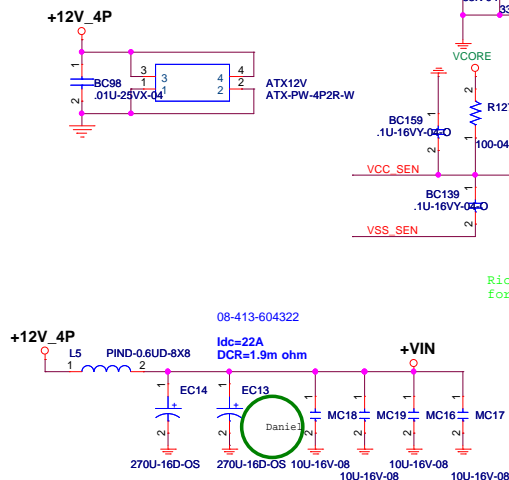
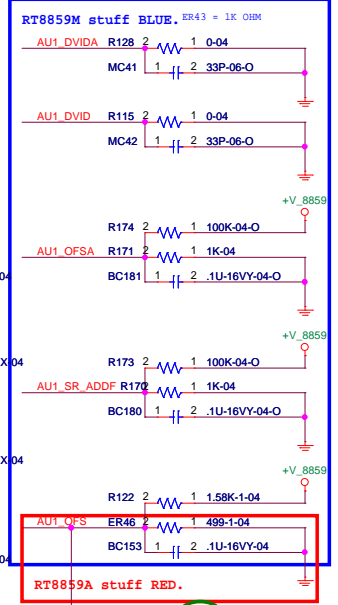
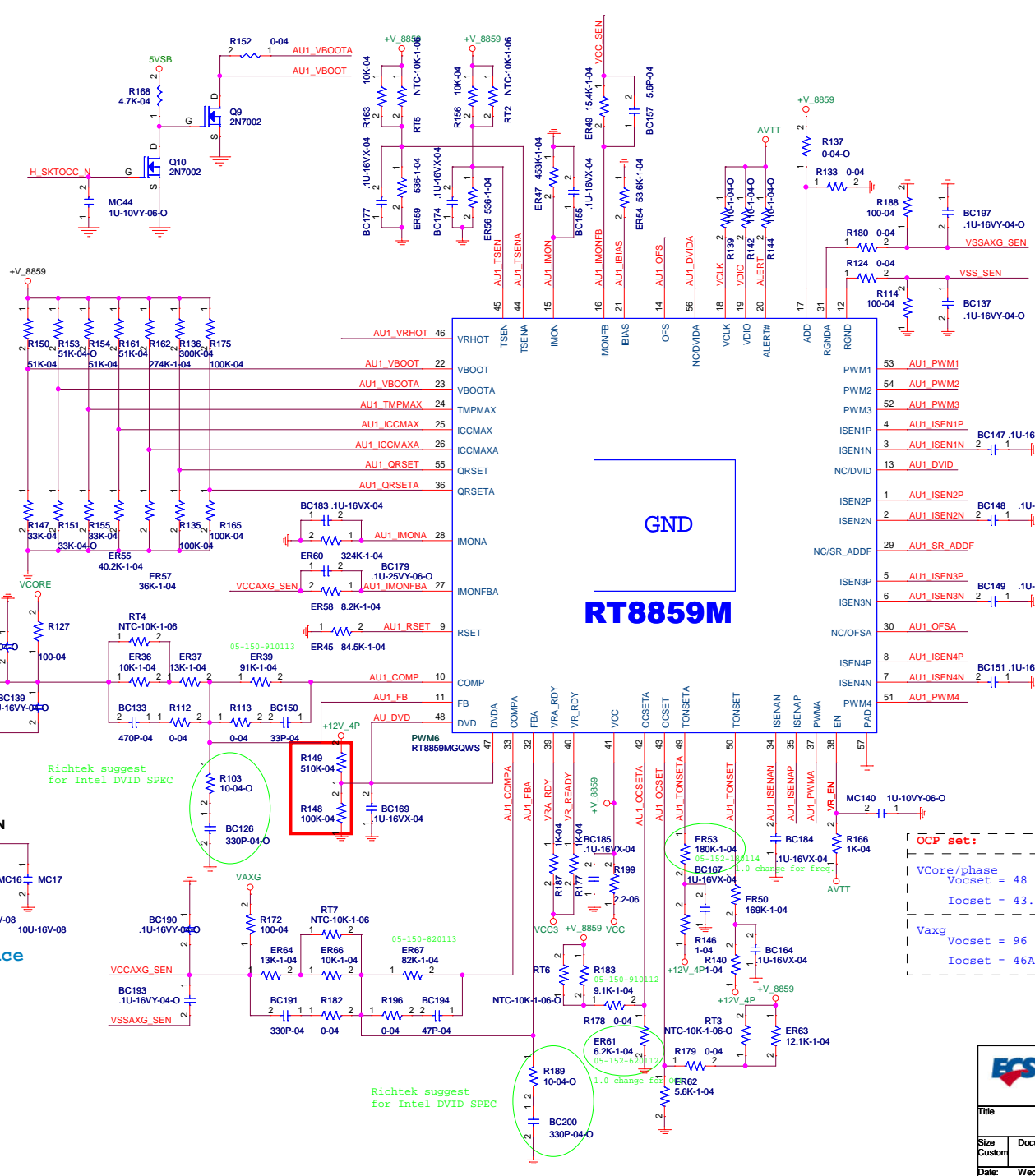
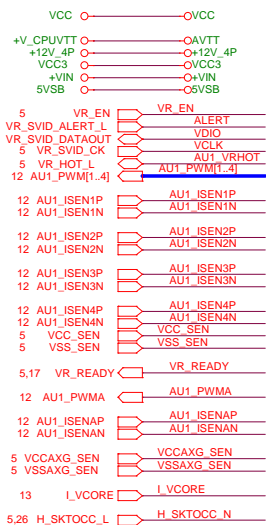








External Connection



OCp set:

VCore/phase

Vocset = 48 * Iocset * Rsense (DCR)

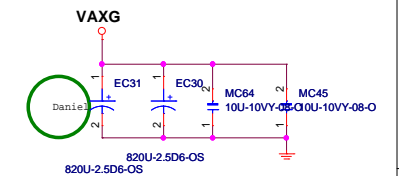
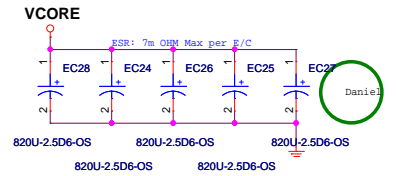
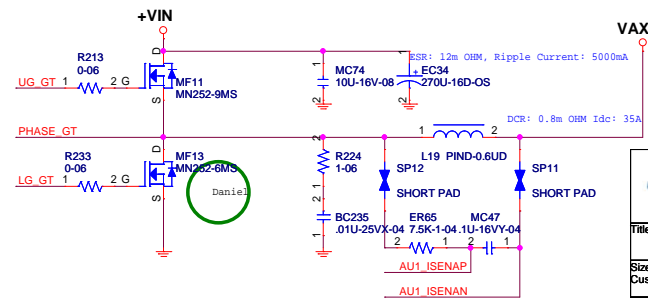
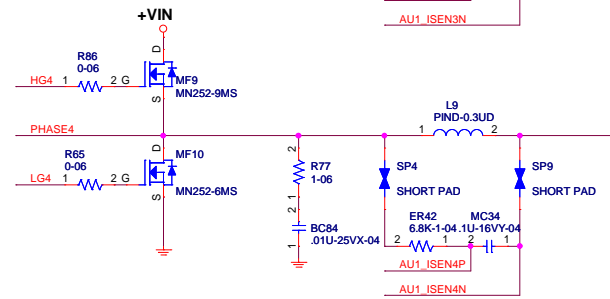
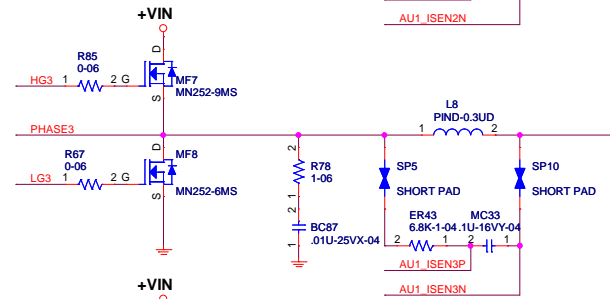
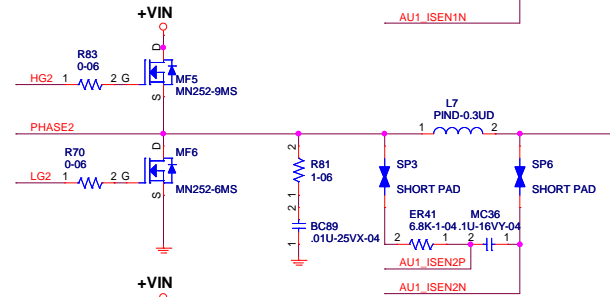
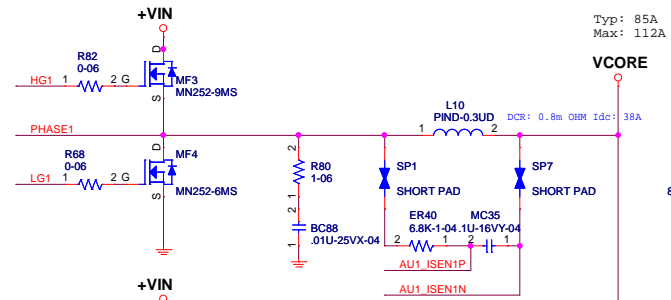
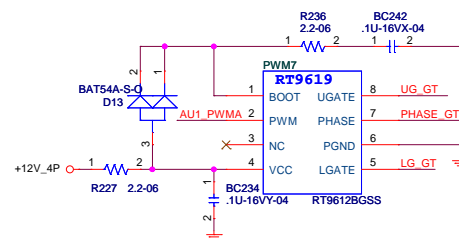
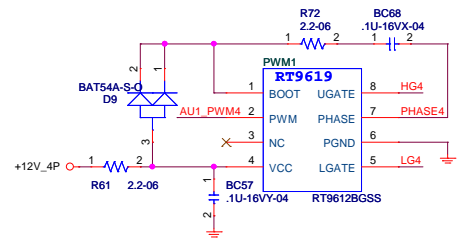
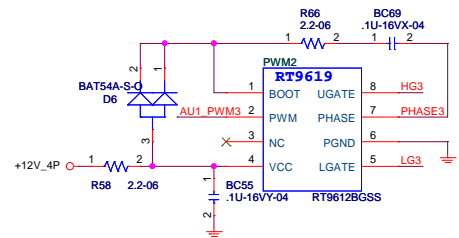
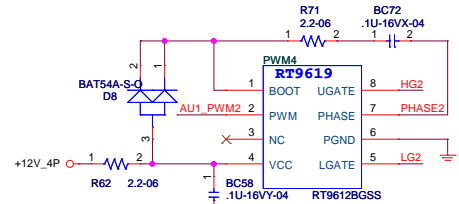
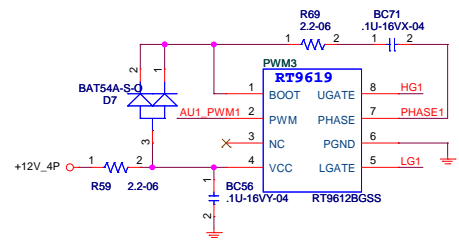
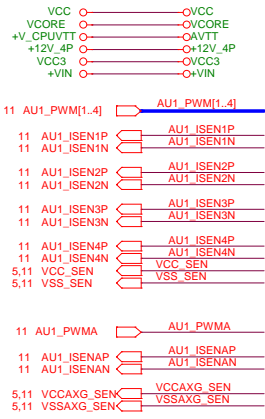
Iocset = 43.35A


Vaxg

Vocset = 96 * Iocset * Rsense (DCR)

Iocset = 46A

External Connection



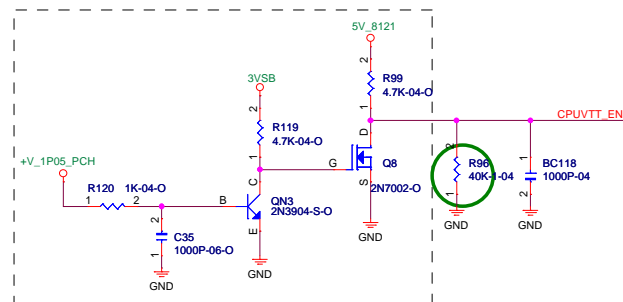
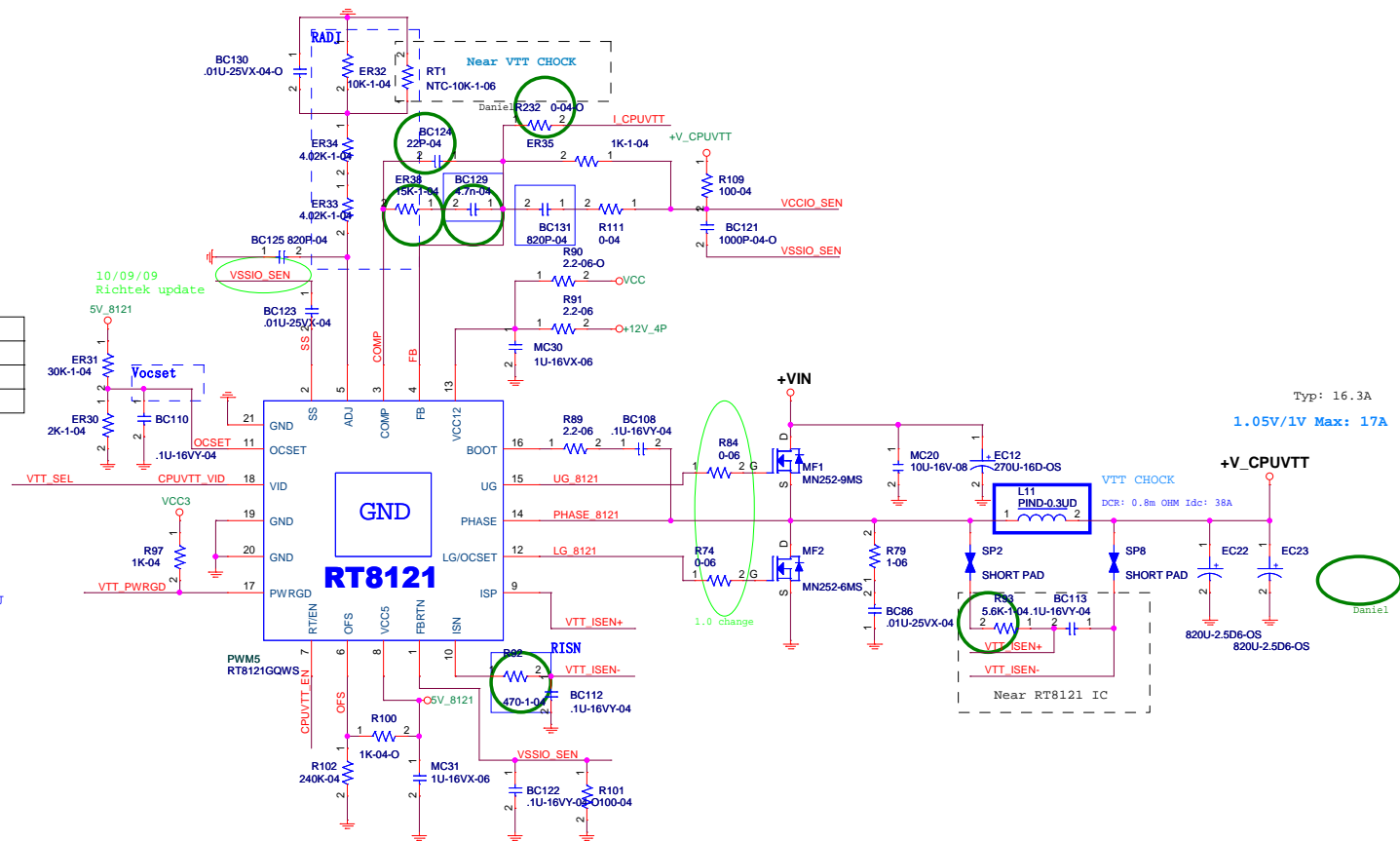
		
VCORE & VAXG / RT9612		
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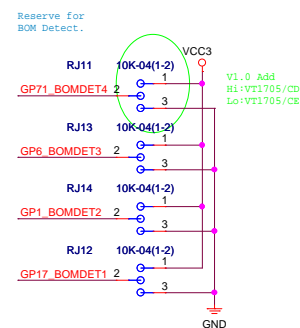


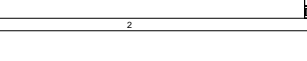
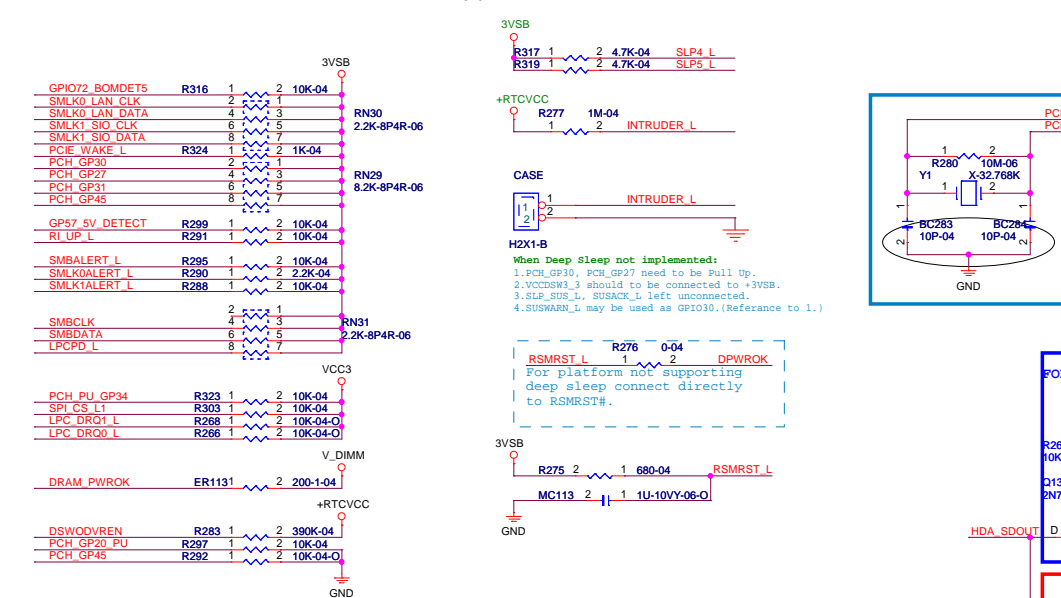
A diagram showing the pin-to-pin connections for the module. It consists of two vertical columns of pins, each with a label to its left. The labels are: VCC, +12V_4P, 3VSB, 5VSB, +V_1P05_PCH, and +V_CPUVTT. Each label is connected to a pin on the left column by a green line. Each pin on the left column is connected to a corresponding pin on the right column by a red line. The right column pins are also labeled with the same text: VCC, +12V_4P, 3VSB, 5VSB, +V_1P05_PCH, and +V_CPUVTT.

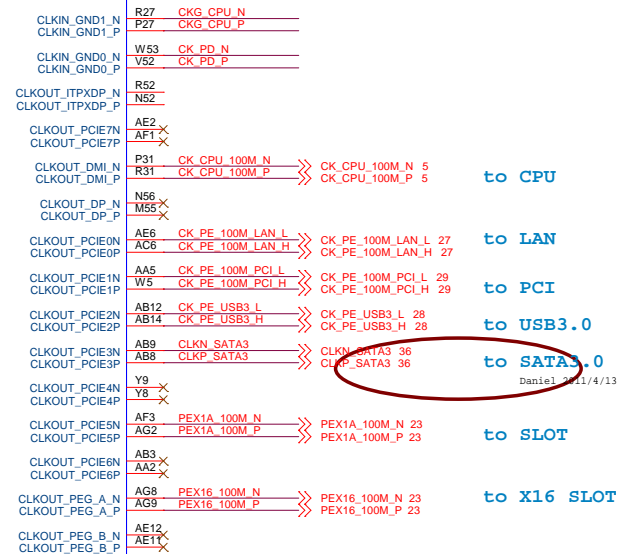
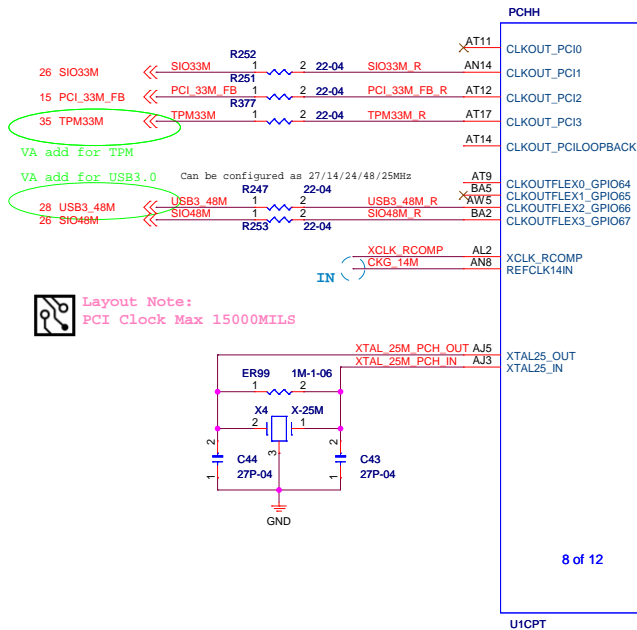
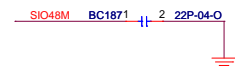
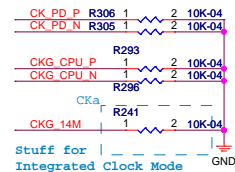
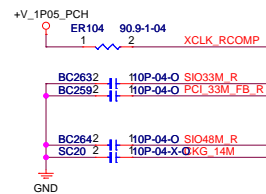


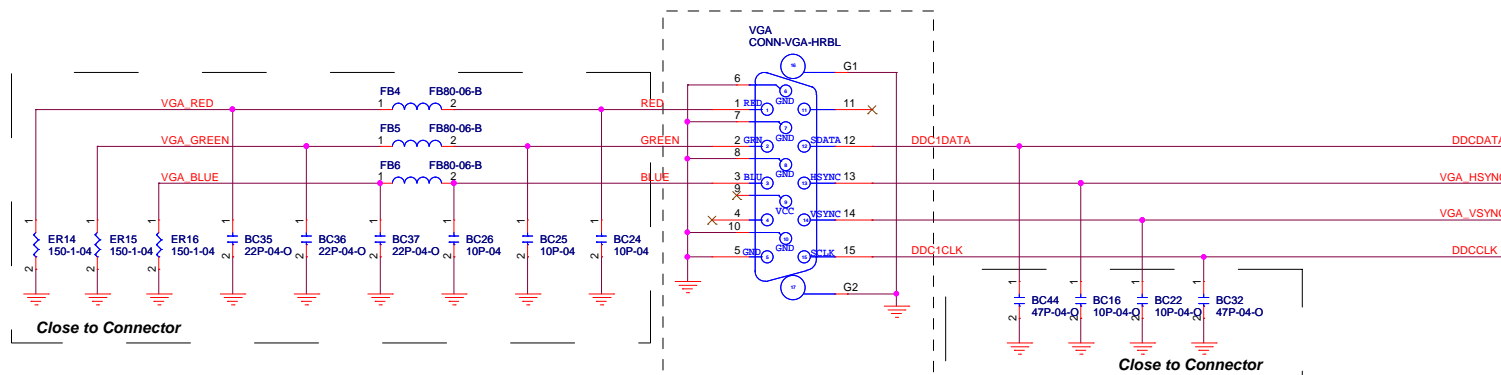
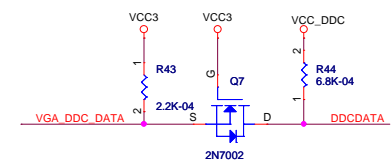
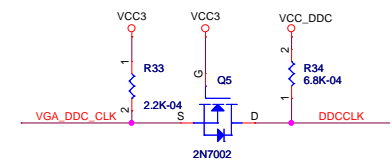
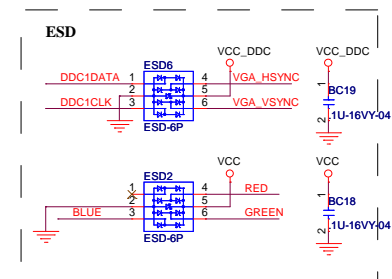
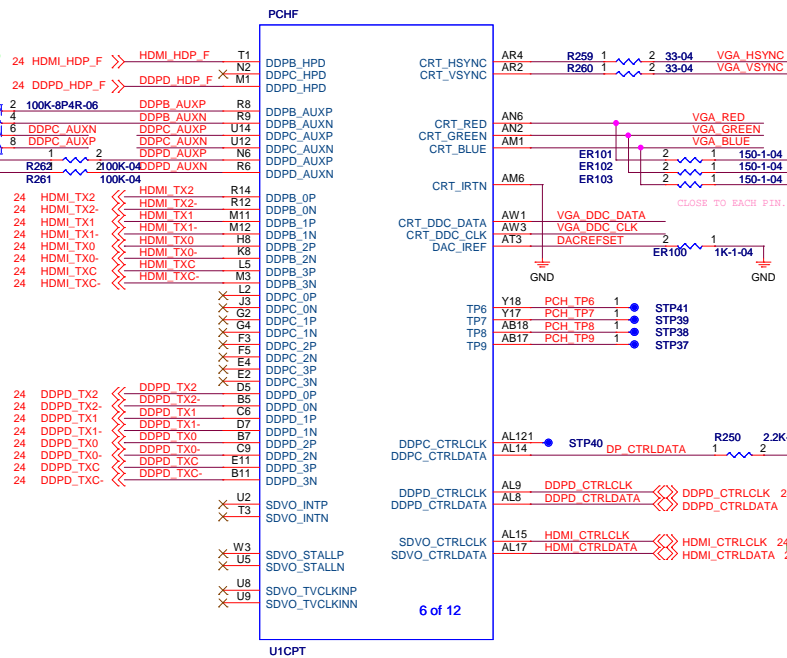
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

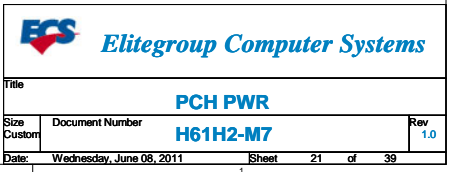
$$\begin{aligned} \text{Vocset} &= \frac{1}{2} * I_x * \text{RADJ} \\ &= \frac{1}{2} * (I_L * \text{DCR} / \text{RISN}) * \text{RADJ} \\ \text{Iocset} &= 31.7\text{A} \\ &= 1.82 * I_{\text{max}} \end{aligned}$$


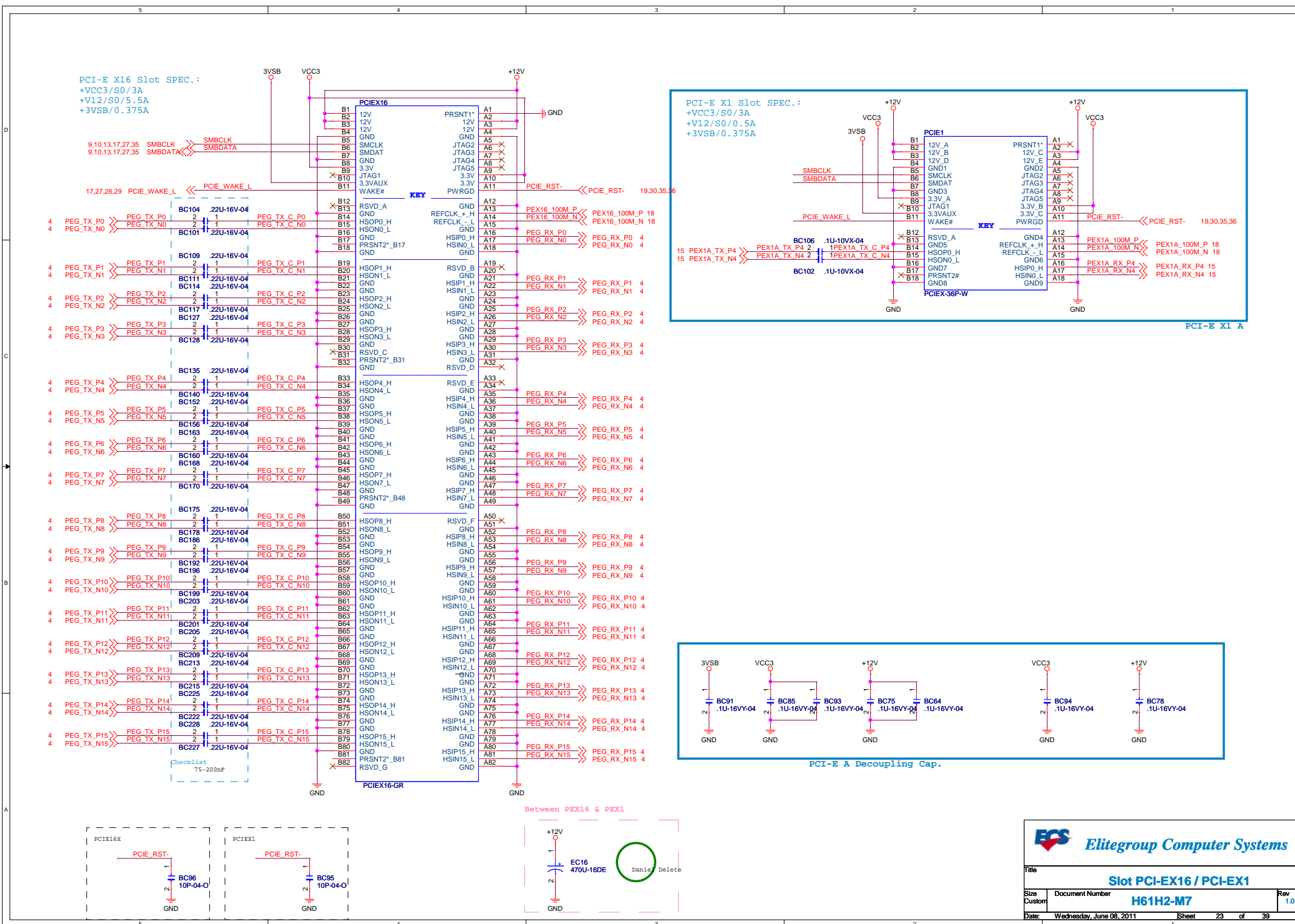




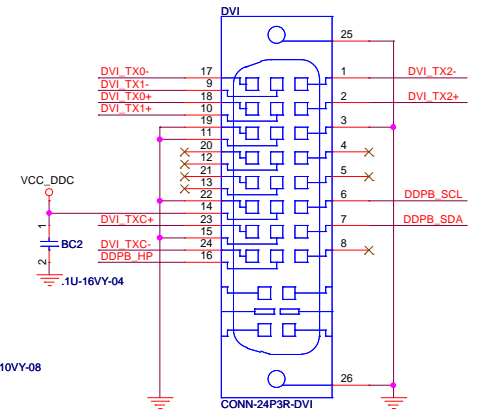
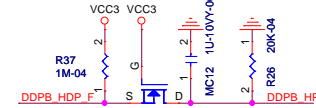
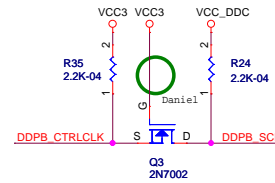
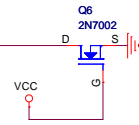
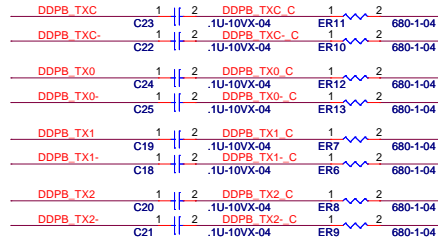
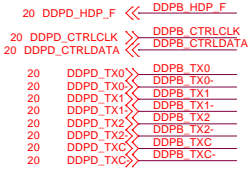




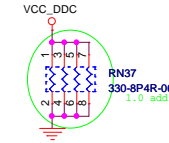
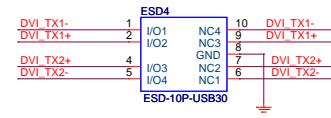
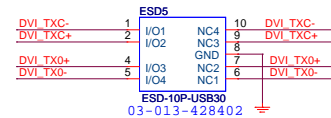
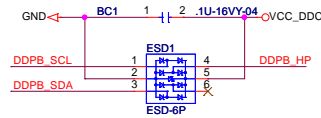
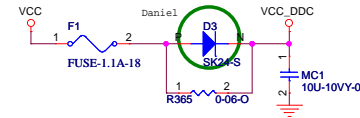
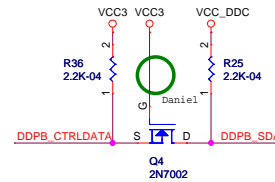
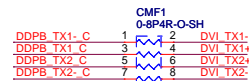
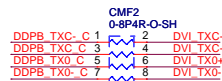




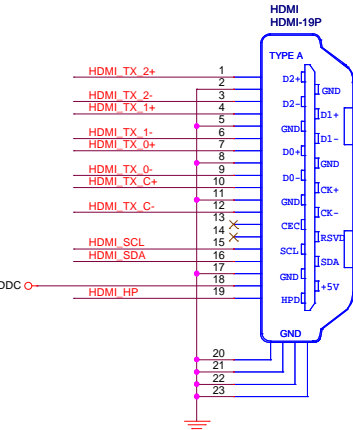
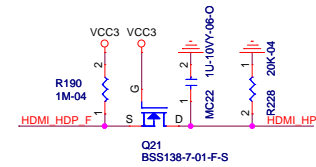
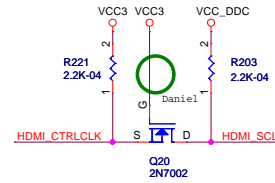
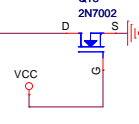
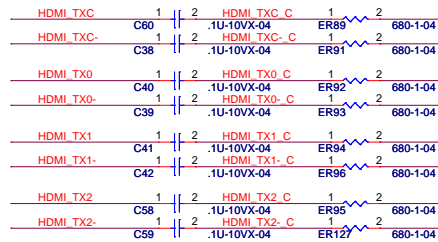
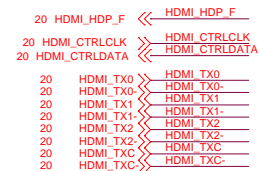
External Connection



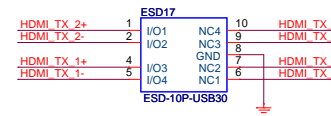
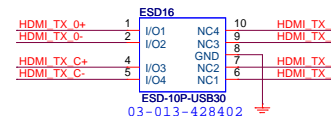
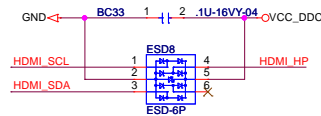
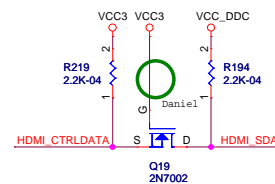
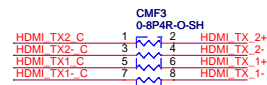
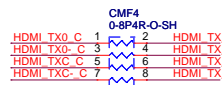
DVI



External Connection

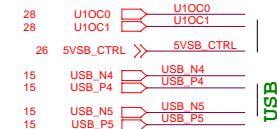
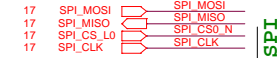
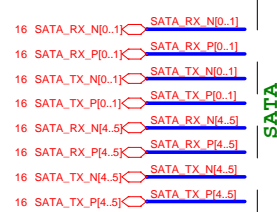
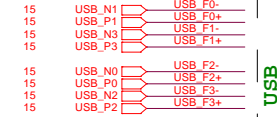
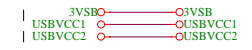


HDMI



Title		
DVI / Rear USB		
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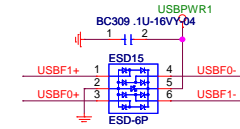
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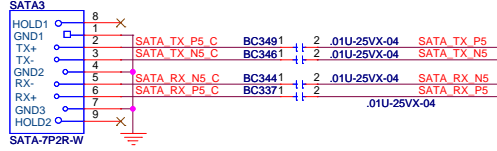
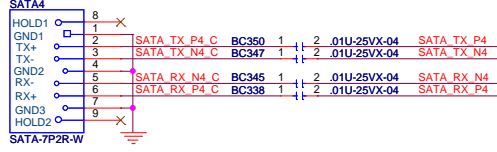
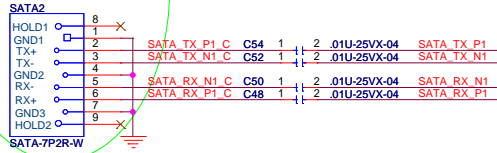
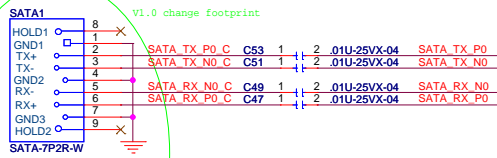
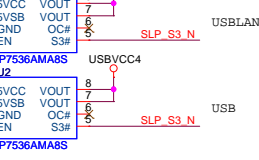
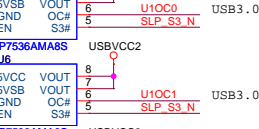
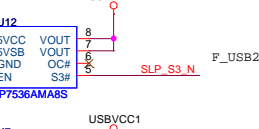
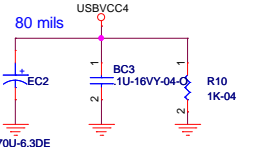
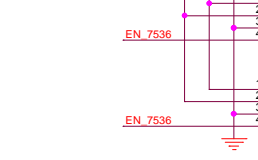
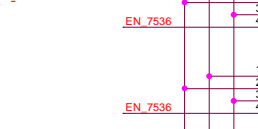
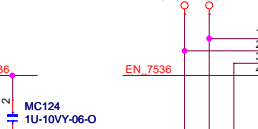
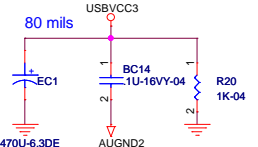
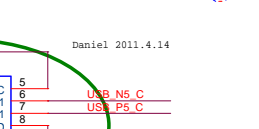
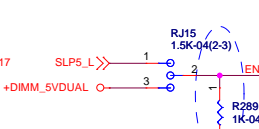
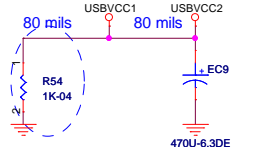
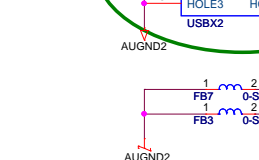
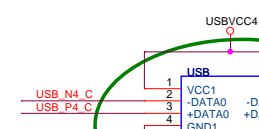
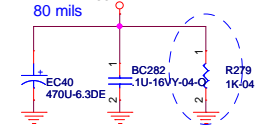
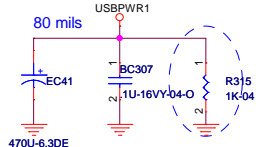
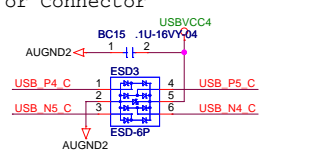
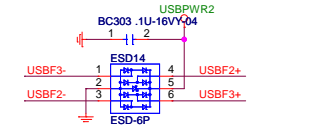
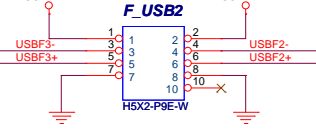
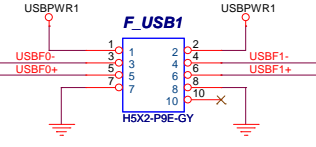
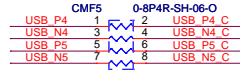
FRONT_SIDE



FRONT_SIDE



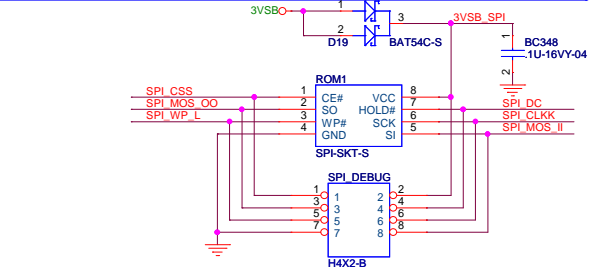
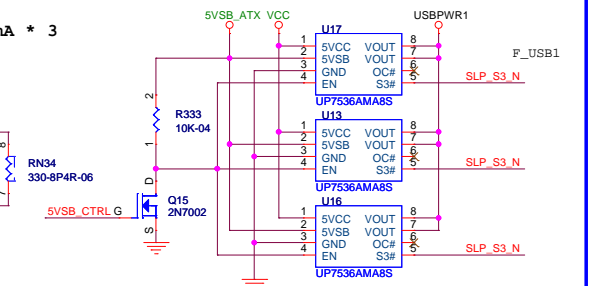
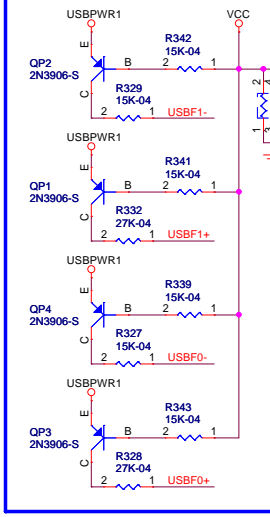
Close to Header or Connector



Layout Note:
SATA3.0 4.5/7.5/20 in 90
Q ±17.5%
SATA2.0 4.5/7.5/15 in 90
Q ±17.5%

Easy Charge

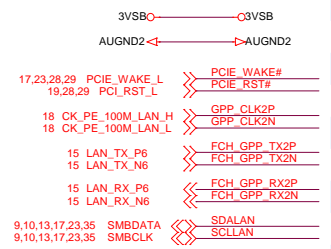
S5 Typ current: 750 mA * 3



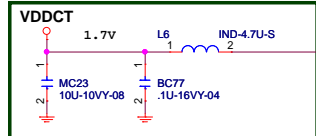
Elitegroup Computer Systems

F_USB / SATA / SPI		
Size	Document Number	Rev
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Date:	Wednesday, June 08, 2011	Sheet 25 of 39

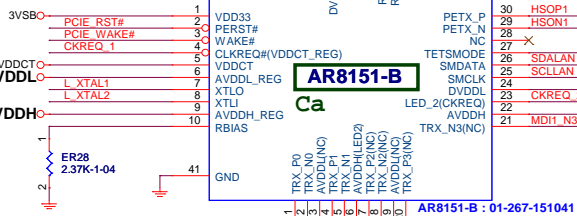
External Connection



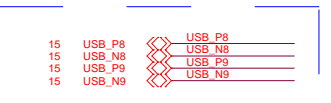
Cb



Ca



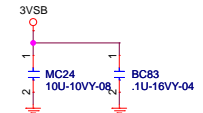
PCH USB2.0



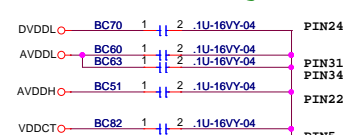
BOM Difference

	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

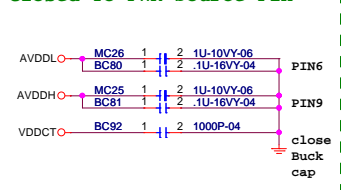
Closed To Pin1



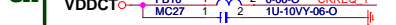
Closed To PWR Loading Pin



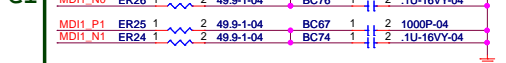
Closed To PWR Source Pin



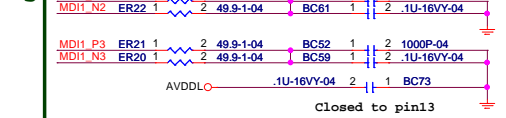
Ch



Ci



Cg

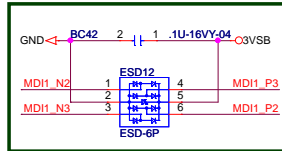


HW Strapping(LED1 for 10/100)

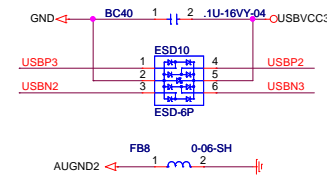
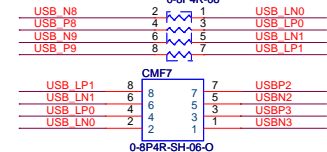
LED0 : 0 -> OC disable
1 -> OC enable
LED1 : 0 -> LDO mode
1 -> SWR mode



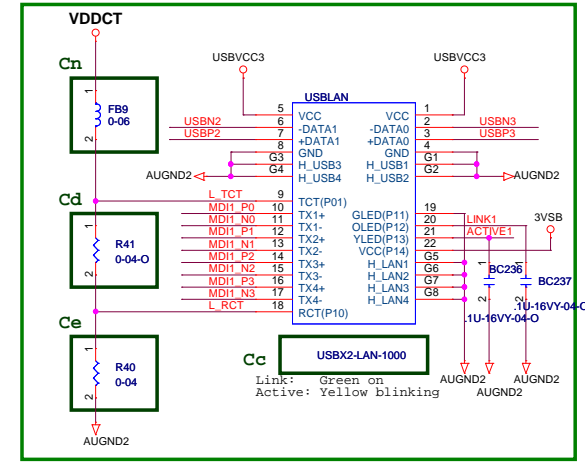
Cf



USB2.0



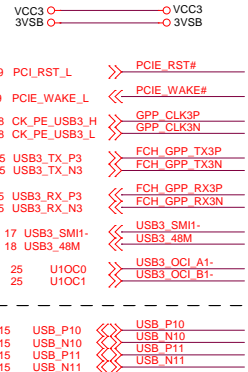
Daniel



Elitegroup Computer Systems

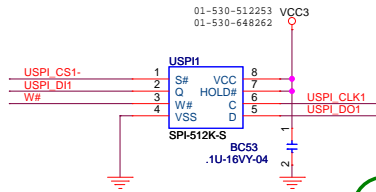
PCIE LAN / AR8151-B		
H61H2-M7		
Size Custom	Document Number	Rev 1.0
Date: Wednesday, June 08, 2011	Sheet 27 of 39	

External Connection

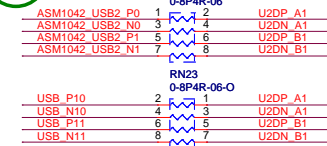


PE_CLKREQ#
PECLKREQ for power saving when PESEL=Low

USB2.0



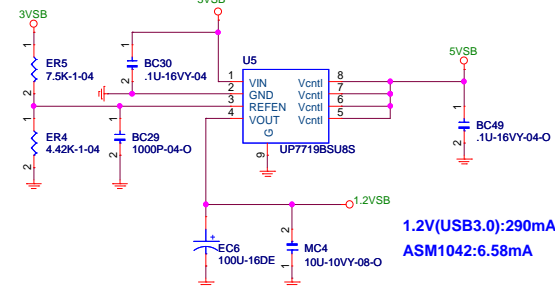
USB2.0



USB3.0



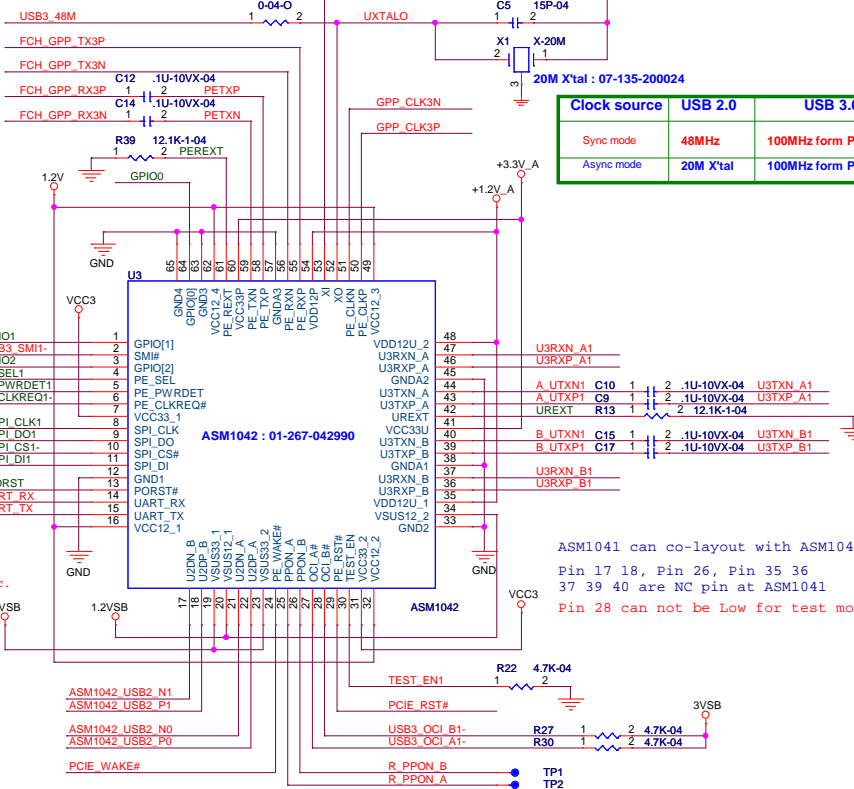
1.2VSB(USB3.0)



1.2V(USB3.0):290mA

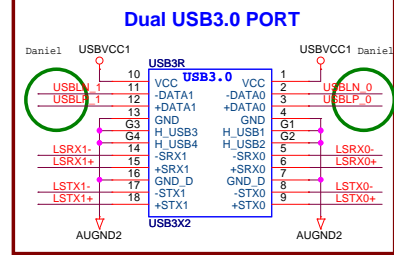
ASM1042:6.58mA

Clock source must follow Rise/fall time less than 2.7ns or slew rate fast then 1ns/V



Clock source	USB 2.0	USB 3.0
Sync mode	48MHz	100MHz form PCIE CLK
Async mode	20M X'tal	100MHz form PCIE CLK

ASM1041 can co-layout with ASM1042
Pin 17 18, Pin 26, Pin 35 36
37 39 40 are NC pin at ASM1041
Pin 28 can not be Low for test mode.



HW Strapping

NET Name	GPIO0/GPIO1/GPIO2
HI	H/H/L=Asynchronous Mode
LO	H/H/L=Asynchronous Mode
	L/L/X=Debug/Test Mode
	Internal Pull-High

NET Name	HI	LO
PESEL1	Others	ExpressCard or MiniCard
PEPWDET1	D3 Cold	D3 Hot



NET Name	HI	LO
PESEL1	Others	ExpressCard or MiniCard
PEPWDET1	D3 Cold	D3 Hot

NET Name	HI	LO
PESEL1	Others	ExpressCard or MiniCard
PEPWDET1	D3 Cold	D3 Hot

NET Name	HI	LO
PESEL1	Others	ExpressCard or MiniCard
PEPWDET1	D3 Cold	D3 Hot

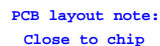
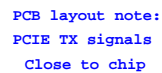
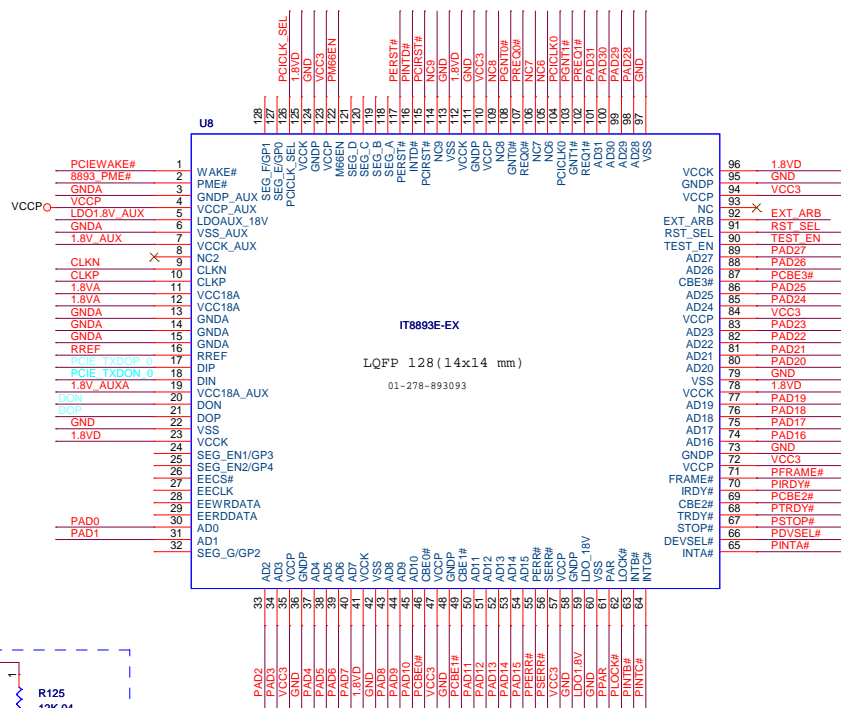
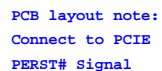
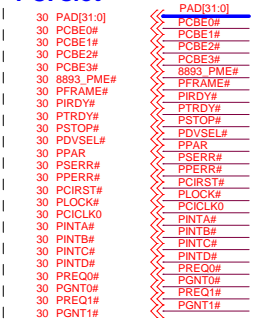
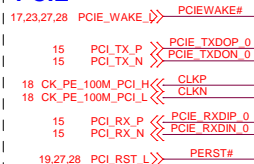
Elitegroup Computer Systems

USB3.0 / ASM1042

Size Custom Document Number H61H2-M7

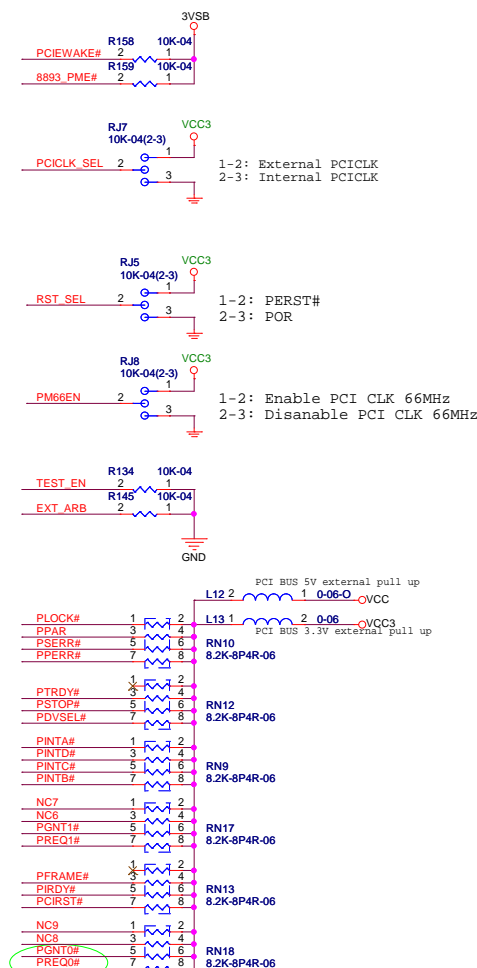
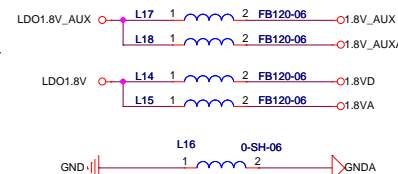
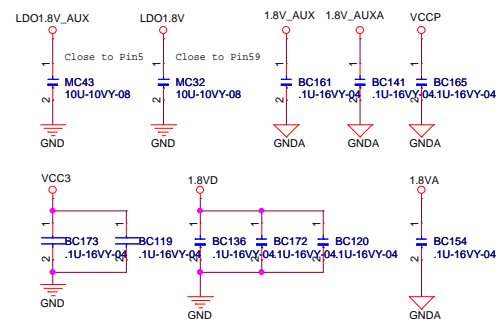
Date: Wednesday, June 08, 2011 Sheet 28 of 39

PCI slot

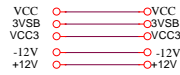


PCIE CLK PCB layout note:

- To meet Differential Impedance :100 ohm +/- 15%
- To meet Single-ended Impedance :50 ohm +/- 15%
- CLKP and CLKN trace width:7 mils
- Space between CLKP and CLKN:14 mils
- L1 & L2 height:5 mils
- The signal traces Number of vias: 4 (Max.)
- The signal trace above analog GND plane
- Spacing from other groups:>25 mils
- Total trace length: 12 inches (Max.)

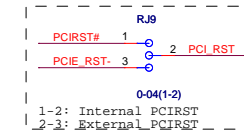
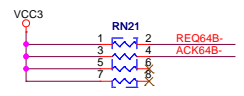
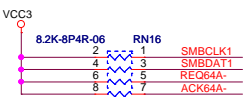
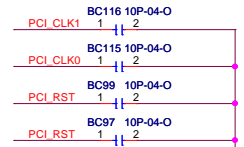
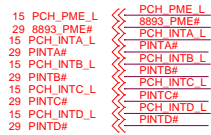
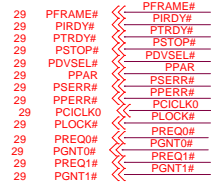


External Connection

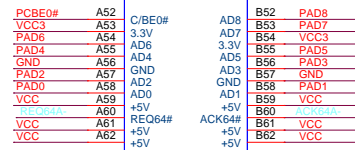
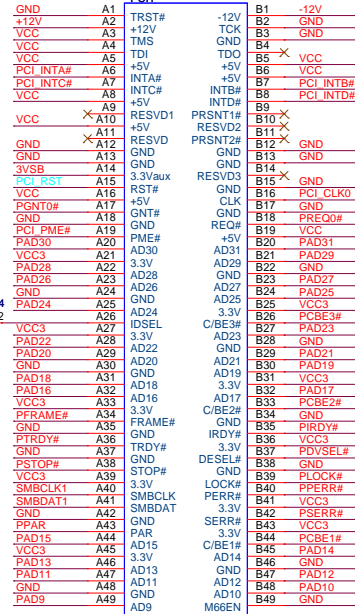


19,23,35,36 PCIE_RST_ PCIE_RST_

COMMON

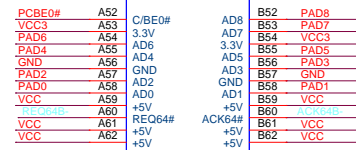
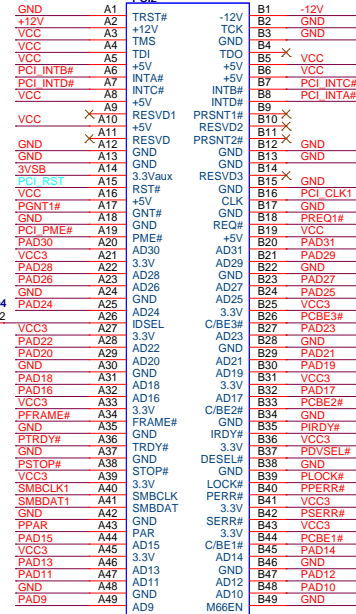


PCI1

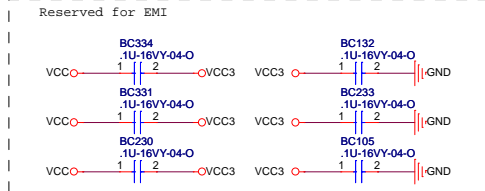
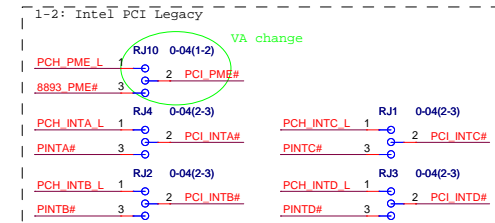
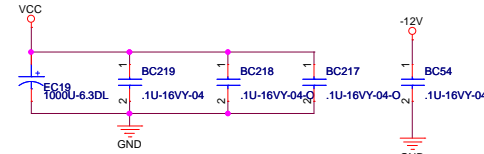
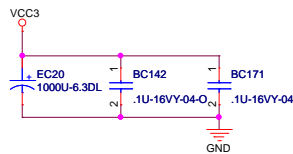


PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

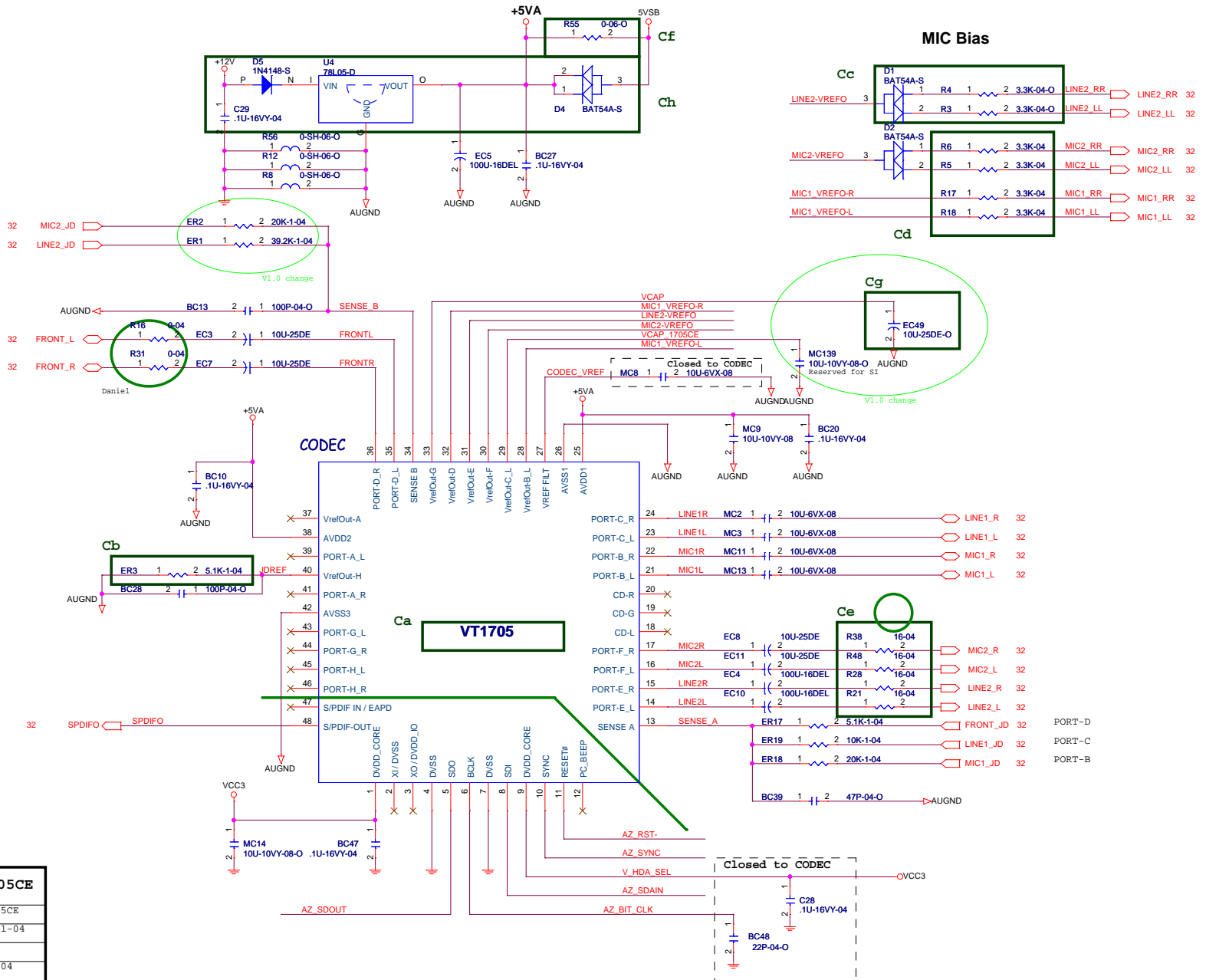
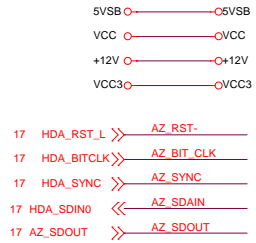
PCI2



PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



External Connection



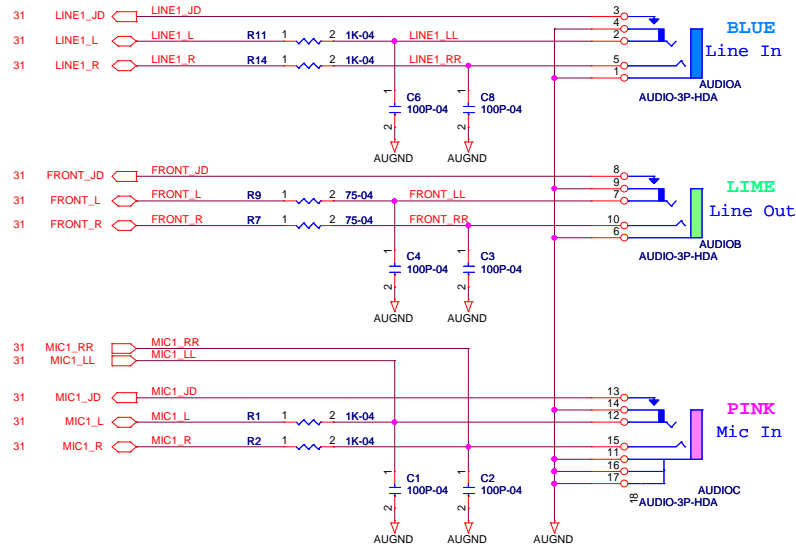
BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

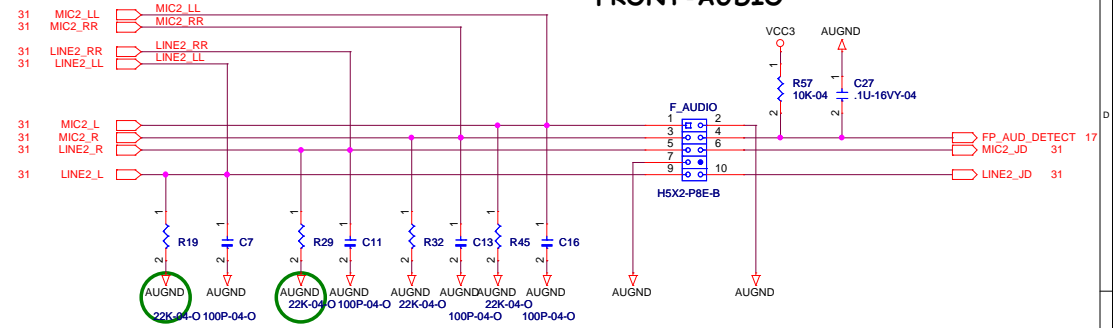
When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

Title			
AUDIO CODEC VT1705			
Size	Document Number	H61H2-M7	
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Date:	Wednesday, June 08, 2011	Sheet	31 of 39

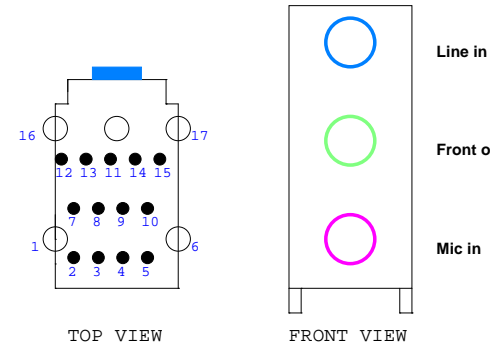
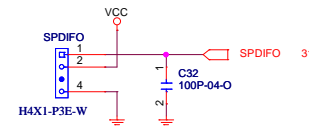
REAR-AUDIO Non re-tasking for rear panel



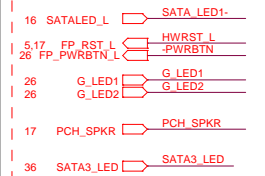
FRONT-AUDIO



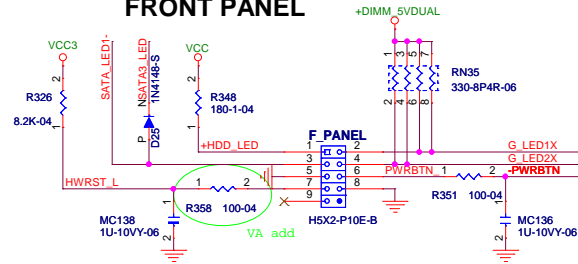
SPDIF-OUT



External Connection



FRONT PANEL

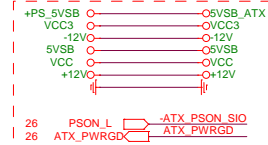


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G_GB	YB	OFF	OFF	OFF	OFF

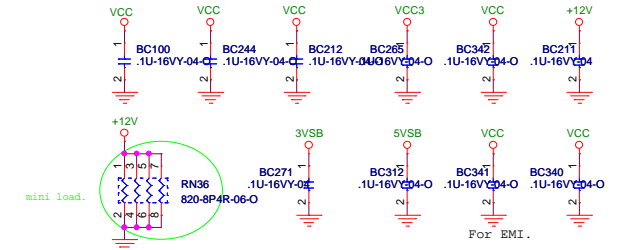
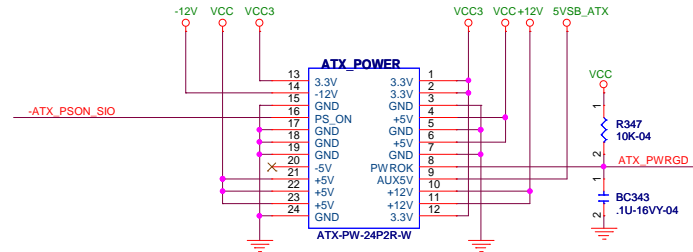
Blinking

POWER CONNECTOR

External Connection



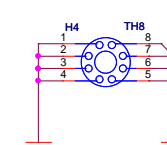
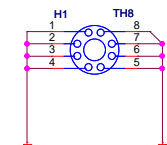
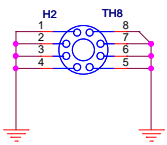
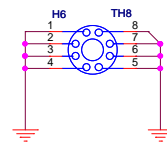
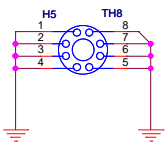
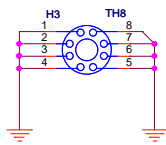
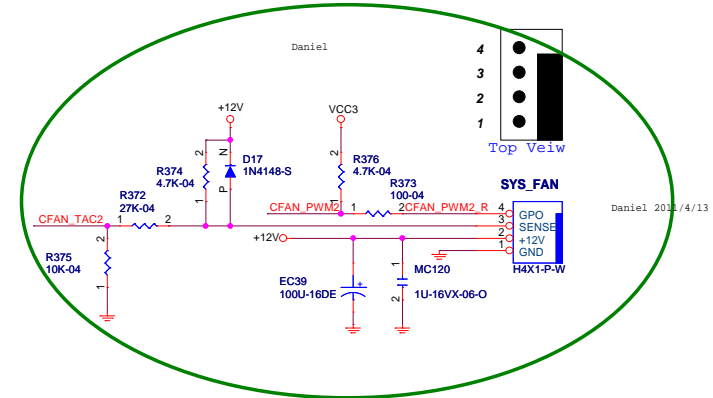
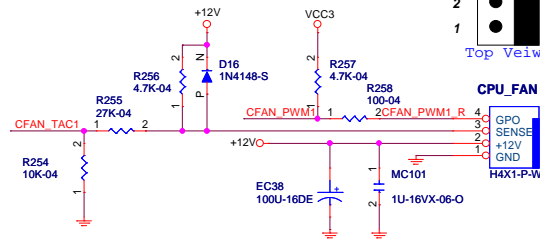
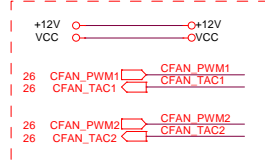
F_PANEL	
+HDDLED	1 2
RST	3 4
	5 6
	7 8
	9



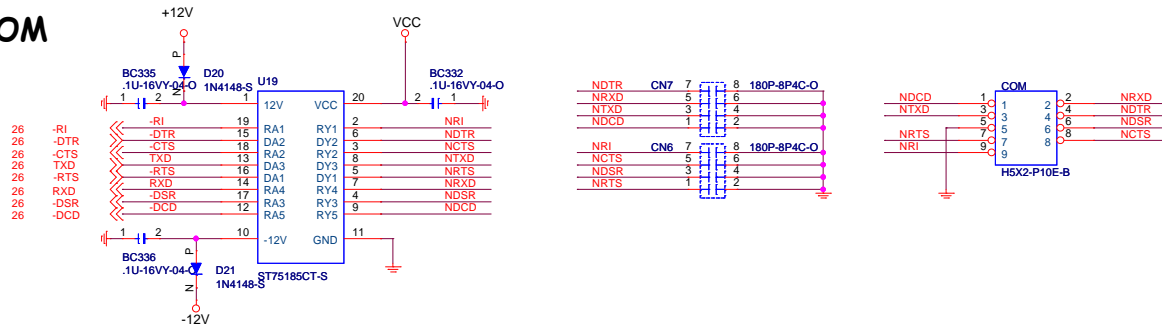
FAN

Kent 1016

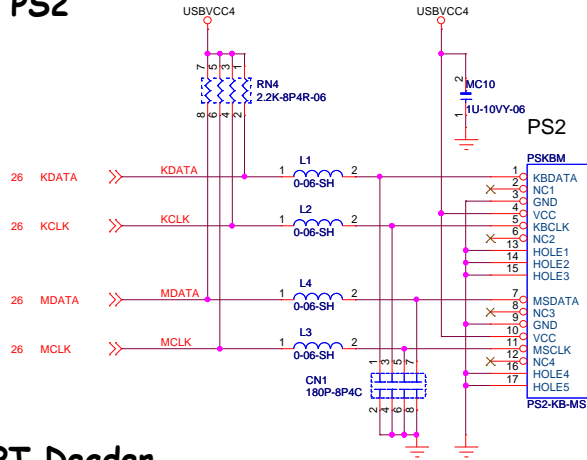
External Connection



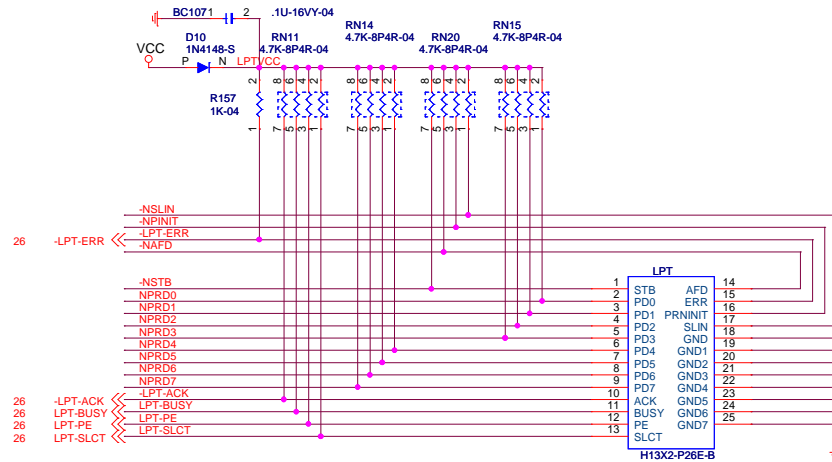
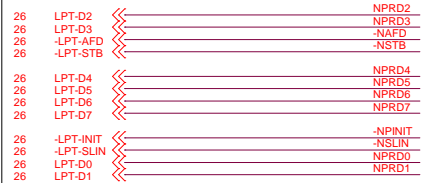
COM



PS2

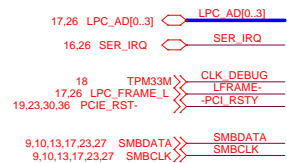


LPT Deader

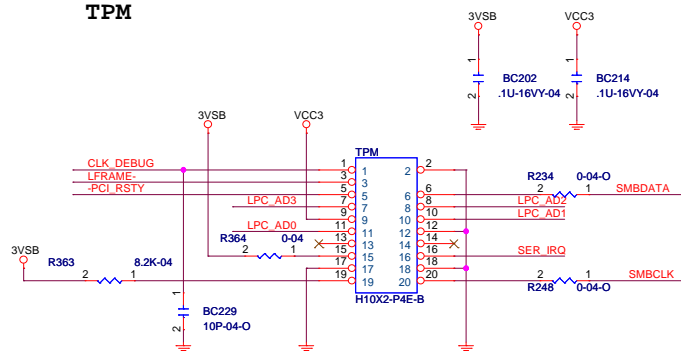


10-342-026387

External Connection



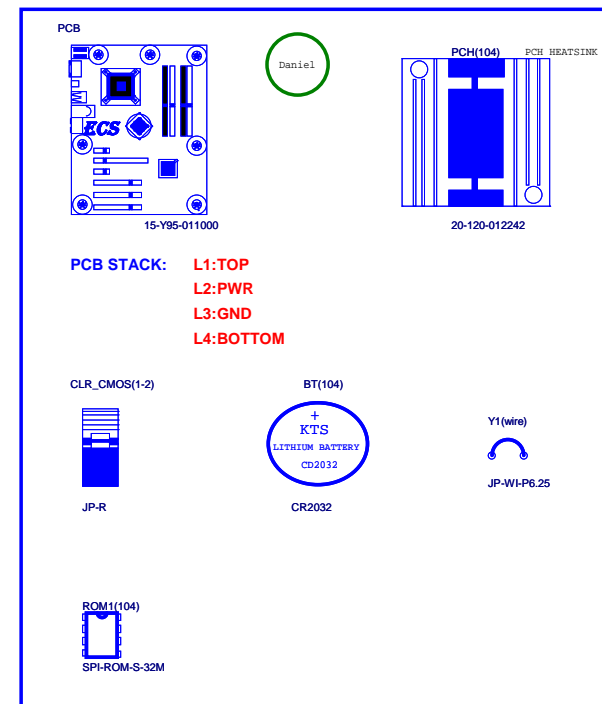
TPM



1)Circuit type 1

Layer 1:TOP	
Layer 2:PWR	
Layer 3:GND	
Layer 4:BOTTOM	

104 Phase



VCC3

33 SATA3_LED

19,23,30,35 PCIE_RST-

18 CLKP_SATA3

18 CLKN_SATA3

15 TXP_SATA3

15 TXN_SATA3

15 RXP_SATA3

15 RXN_SATA3

LED_SATA

PERST_SATA

PECLKP_SATA

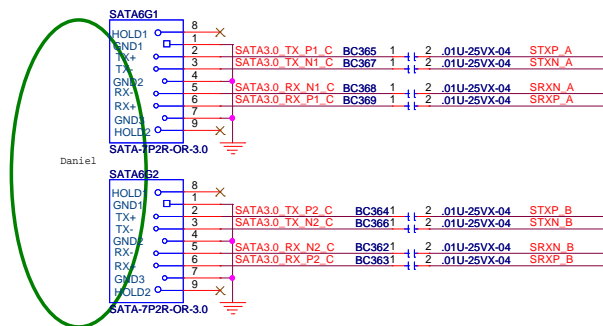
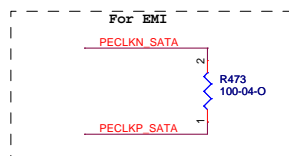
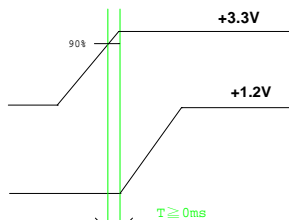
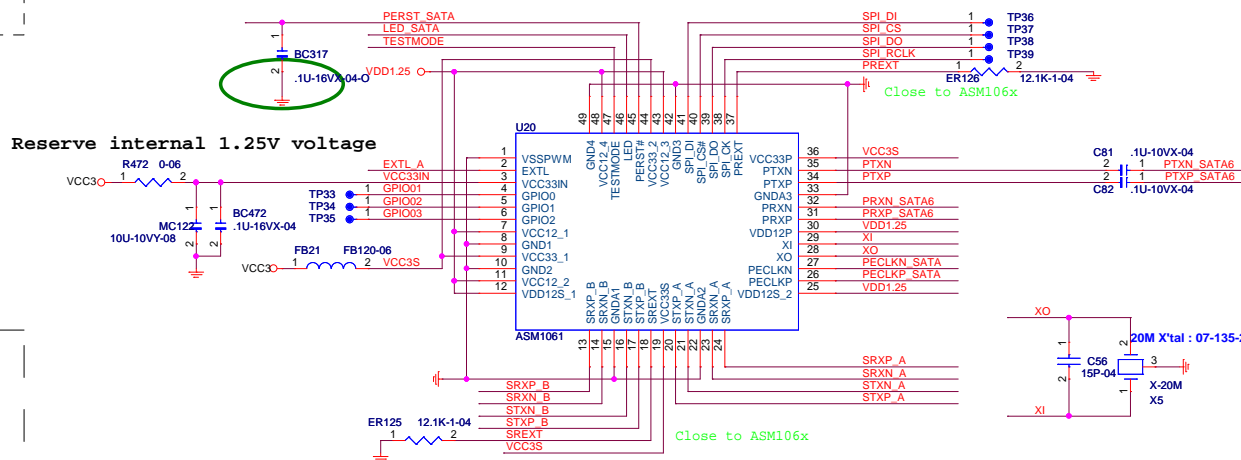
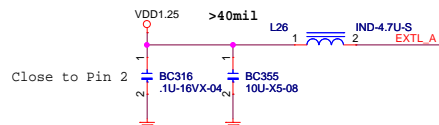
PECLKN_SATA

PRXP_SATA6

PRXN_SATA6

PTXP_SATA6

PTXN_SATA6



SPI_DO R370 2 1 4.7K-04

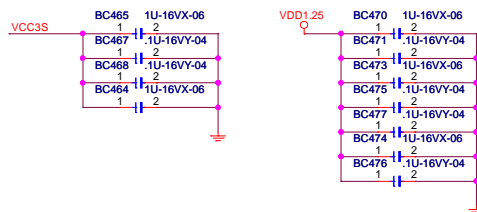
SPI_DO

0: Spinup by H/W
1: Spinup by S/W

TESTMODE R367 2 1 4.7K-04

TESTMODE_10048

0: Disable
1: Enable



ATX P/S WITH 1A STBY CURRENT					
5VSB	5V	3.3V	12V	-12V	
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	

ATX4P	12V	+/-5%
-------	-----	-------

Switching	RT8859A	4 phases
-----------	---------	----------

Switching	RT8121	1 phase
-----------	--------	---------

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S0

LDO	APL5336
-----	---------

Linear	OP358
--------	-------

Intel Sandy Bridge CPU		
VCCP	V _{DD} 0.25~1.52V	85A(95W)
VAXG	V _{DD} 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V _{PROC_IO}	1.05V	1mA
V _{ccDMI}	1.05V	0.057A
V _{ccCORE}	1.05V	1.6A
V _{ccIO}	1.05V	4.07A
V _{ccADPLLA}	1.05V	0.1A
V _{ccADPLLB}	1.05V	0.1A
V _{ccCLKDMI}	1.05V	0.02A
V _{ccSSC}	1.05V	0.105A
V _{ccDIFFCLKN}	1.05V	0.055A
V _{ccASW(ME)}	1.05V	1.61A
V _{ccDFTerm}	1.8V	0.2A
V _{ccVRM}	1.8V	0.159A
V _{cc3_3}	3.3V	0.409A
V _{ccADAC}	3.3V	0.068A
V _{ccSPI}	3.3V	0.02A
V _{ccDSW3_3}	3.3V	0.003A
V _{ccSUS3_3}	3.3V	0.097A
V _{ccSUSHDA}	3.3V	0.01A
V _{ccRTC}	3.3V	6uA(G3)
V _{5REF}	5V	1mA
V _{5REF_SUS}	5V	1mA

Fans	12V_200mA
------	-----------

SPI	VCC3_30mA
-----	-----------

CRT	VCC_1A fuse
-----	-------------

HDMI/DP	VCC3_0.5A fuse x 2
---------	--------------------

HDMI L.S.	VCC3_180mA
-----------	------------

Flash/NVM	VCC3_0.3A
	1.8V_0.1A

NEC_D720200		
VDD3P3	3.3V	TBD
VDD1P05	1V	TBD
CTRL1P0 internal LVR Output		

SUPER I/O IT8728		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC892		
+5V SD	5V	0.01A
+5V	5V	0.1A

Battery 3V

X16 PCIe Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A
Total 1 Slot	

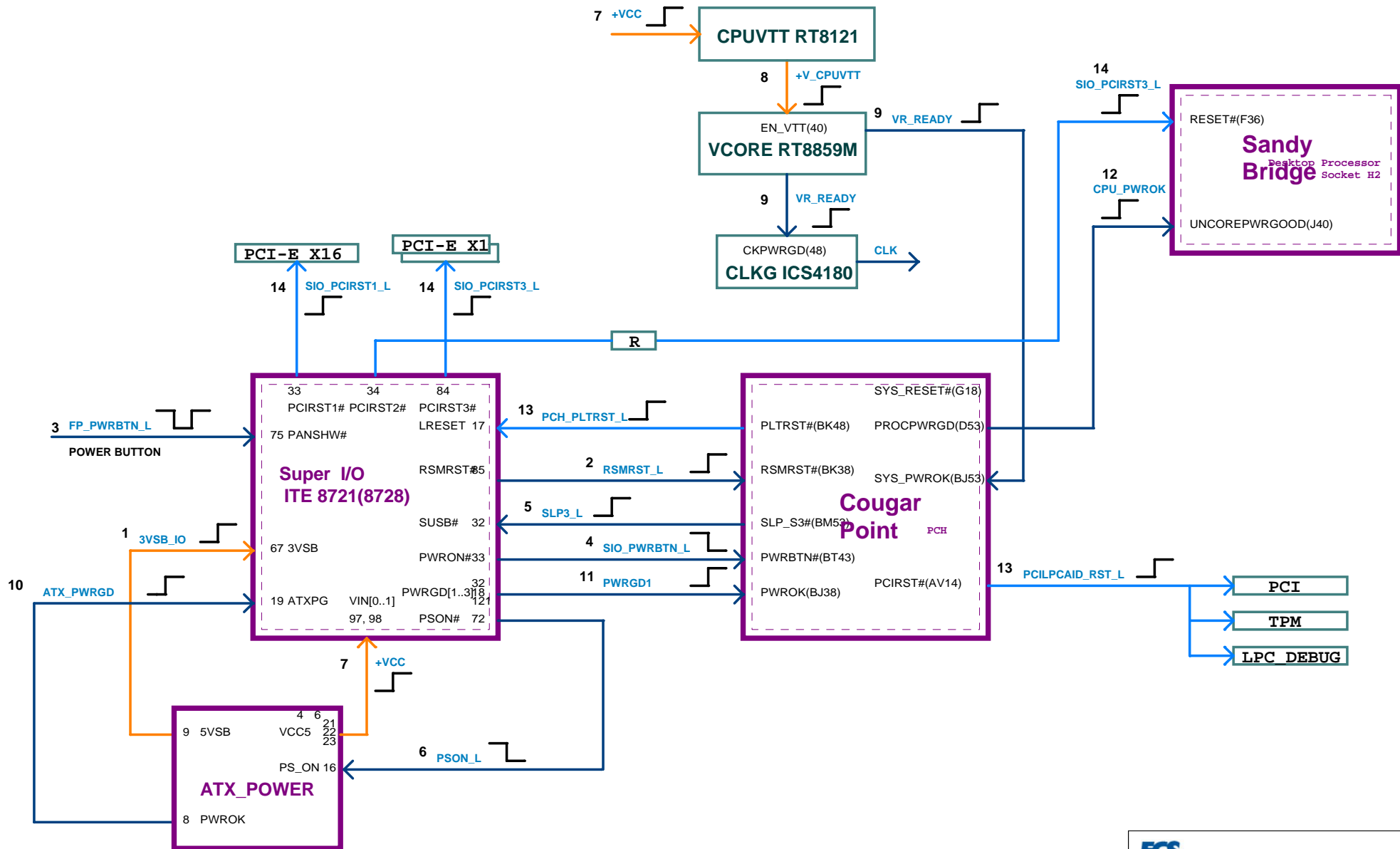
X1 PCIe Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
Total 1 Slots	

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)
Total 2 Slot	

USB X4 Header	
VDD	5VDual
2.0A	2.0A

USB X4 IO	
VDD	5VDual
2.0A	2.0A

USB3.0	
5VDual	2A



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

